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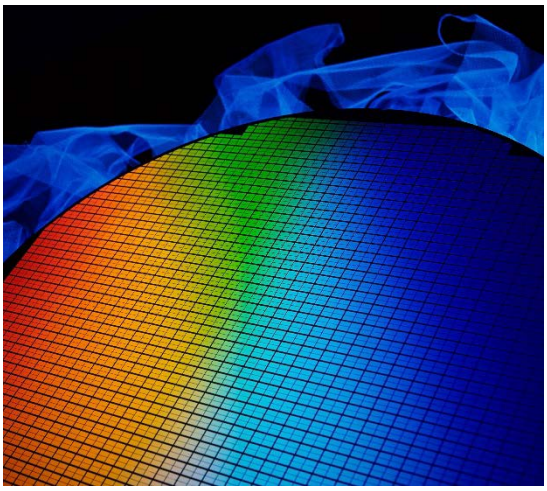


Semiconductor Technology Trend and Reliability Challenges

Speaker, Richard Rao, Ph.D., MicroSemi

Oct 13, 2015 at 6:30 pm

Location: Skyworks Solutions, Newbury Park, CA

Meetings are free and open to the public

RSVP at this link

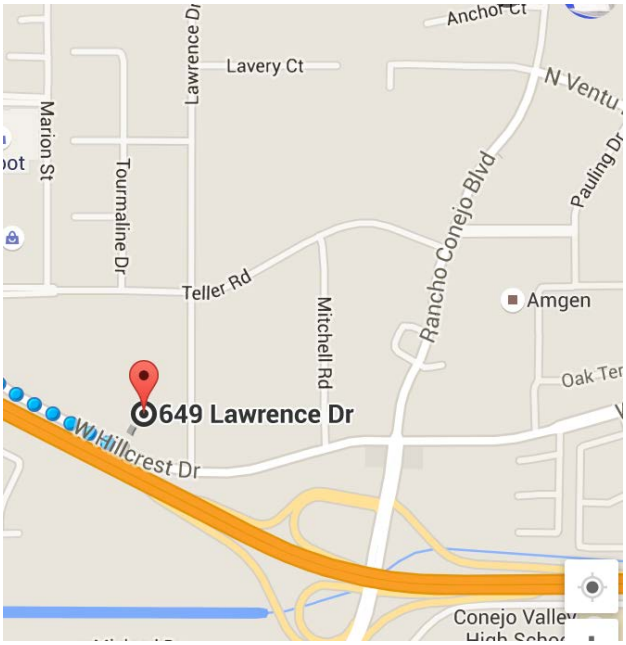
As the IC industry rapidly adopts new semiconductor technologies with increased density and introduces new fabrication methods to enable novel IC structures, chip designers wrestle with a surge of failure mechanisms. It has become necessary to take the art of design for reliability to the next level. This talk will give an overview of reliability failure mechanisms of an advanced IC product focusing on the wafer, the die, the package and their mutual interactions. Dr. Richard Rao will then take the audience onto a few technical deep dives to expose some of the less well understood albeit frequent chip failures. The talk will conclude with the testing required to root out the issues.

Dr. Richard RAO is currently a Microsemi Technical Fellow. He manages the reliability program and focuses on the development of design for reliability (DfR) flows to deal with the challenging reliability failure mechanisms associated with advanced semiconductor process and packaging technology. These include the back end and far back end interconnect Electromigration and Stress Migration; transistor Gate Oxide Breakdown, Hot Carrier Injection and Bias Temperature Instability; and chip to package interaction failures. He has a Ph.D. degree in solid mechanics of materials from the University of Science and Technology of China. Prior to joining Microsemi (Vitesse before April, 2015) in 2004, Dr. Rao held various academic and technical positions in reliability physics and engineering. He was an associate professor at University of Science and Technology of China, a research fellow at Northwestern University, USA and National Science and Technology Board of Singapore. He also held senior and principal engineering positions in Vitesse Semiconductor Corp, JDS Uniphase, Ericsson Inc and Motorola Electronics. He has published about 30 papers on reliability physics and applications and also a main contributor of several JEDEC standards. He is a conference and session keynote speaker at International Conference on Electronics Packaging Technology and a technical committee member for International Reliability and Physics Symposium. He has given numerous talks at various conferences such as IRPS (International Reliability and Physics Symposium), ECTC (Electronics Component and Technology Conference), ISQED (International Symposium on Quality Electronics Design), ASME Symposiums and ICEPT, etc. Dr. Rao has over 20 years of experience and knowledge in the advanced Si processes including 65nm and beyond nodes, flip chip and 2.5D TSV packaging, chip to package interaction, board and system level reliability physics and applications. He has conducted professional development courses on advanced IC to many engineers in both IC suppliers and users.

Location

Skyworks Solutions
649 Lawrence Drive, Newbury Park, CA 91320
Intersection of West Hillcrest Drive and Lawrence Drive
(not the main building, please use link below to arrow that pinpoints building)
http://maps.google.com/maps?q=34.187542,-118.930994&num=1&t=h&vpsrc=0&ie=UTF8&z=18&iwloc=A

Directions



From Los Angeles

Highway 101 North
Take exit 47A for Rancho Conejo Blvd
Use the left lane to turn right onto Rancho Conejo Blvd
Turn left onto W Hillcrest Dr.
Destination will be on the right

From Ventura

Highway 101 South
Take exit 47B for Wendy Dr. toward Newbury Park
Turn right onto N Wendy Drive
Continue onto Camino Dos Rios
Turn right onto W Hillcrest Drive
Destination will be on the left.