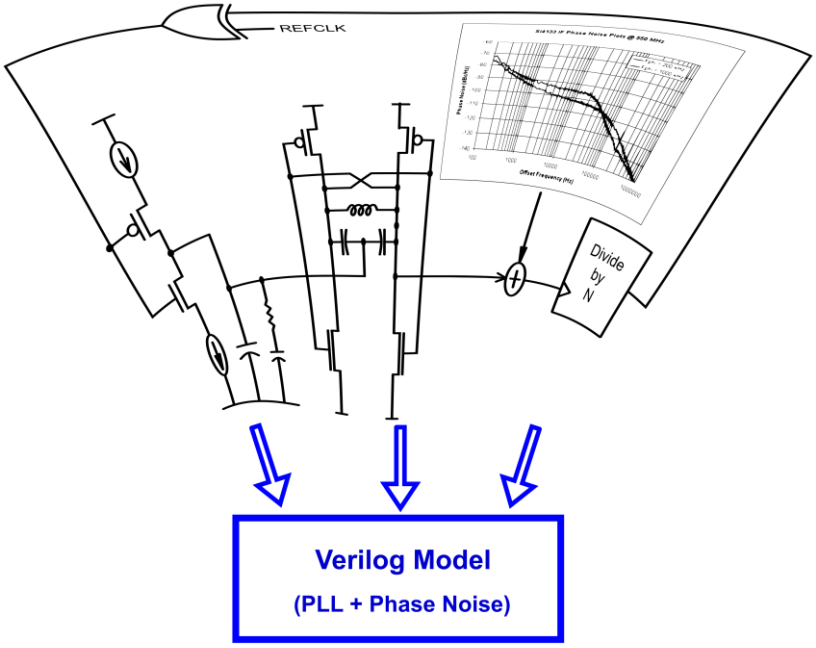
BUENAVENTURA ELECTRON DEVICES / CIRCUITS AND SYSTEMS SOCIETIES CHAPTER

PLL's and Phase Noise Modeling in Verilog

Speaker: Greg Warwar, Teradyne, Inc., Agoura Hills, CA 91301

May 22, 2018 at 6:30 PM

Location: Skyworks Solutions, Newbury Park, CA



Verilog is the accepted language of choice for modeling and simulating digital designs. For analog blocks the tool choice is a low level circuit simulator like HSPICE or Spectre. For PLL's a common misconception is that you can use Verilog to model a PLL if you don't care about accuracy, but if you do care about precision, you'll need an analog circuit simulator like HSPICE or Spectre. Various options like Verilog-A and Verilog-AMS are attempts to achieve the best of both worlds, but in this talk, we propose that the tool of choice for modeling and studying PLL's and is plain "digital" Verilog. It's the right tool, but almost always used the wrong way for modeling PLL's. Understanding how the underlying simulation engine in Verilog works enables us to set up our models in a very precise, yet very simple manner. The efficiency and speed of Verilog allows us to literally watch our PLL designs come alive in the time domain with timing accuracy that can't be achieved in an analog circuit simulator. Watching designs operate in the time domain crystalizes our understanding of them, and enables us to study and quantify transient and other non-linear phenomena.

Greg Warwar received a master's degree in electrical engineering from Rice University in 1989. Following graduation, he joined Texas Instruments in Dallas, TX as a member of the technical staff where he worked on ΣΔ analog to digital converters for precision audio applications. In 1992, he joined Vitesse Semiconductor in Camarillo, CA where he worked for 23 years on high speed serial communications IC's, focusing on many areas of analog and mixed-signal design including VCO's, phase locked loops, clock recovery, frequency synthesizers, and adaptive equalization. Since 2015, Greg has been a principal engineer in the mixed-signal ASICs design group at Teradyne, Inc. in Agoura Hills, CA. Greg holds six U.S. patents in the area of CMOS mixed-signal IC design.

Location

Skyworks Solutions

649 Lawrence Drive, Newbury Park, CA 91320

Intersection of West Hillcrest Drive and Lawrence Drive

(**NOT** the main building, please use link below to arrow that pinpoints building)

http://maps.google.com/maps?q=34.187542,-118.930994&num=1&t=h&vpsrc=0&ie=UTF8&z=18&iwloc=A

Directions

From Los Angeles

Highway 101 North
Take exit 47A for Rancho Conejo Blvd
Use the left lane to turn right onto Rancho Conejo Blvd
Turn left onto W Hillcrest Dr.
Destination will be on the right

From Ventura

Highway 101 South
Take exit 47B for Wendy Dr. toward Newbury Park
Turn right onto N Wendy Drive
Continue onto Camino Dos Rios
Turn right onto W Hillcrest Drive
Destination will be on the left.