BUENAVENTURA ELECTRON DEVICES / CIRCUITS AND SYSTEMS SOCIETIES CHAPTER

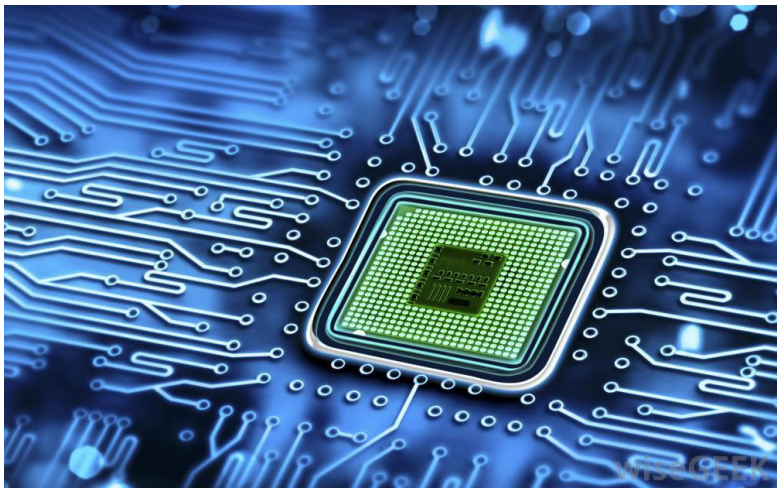
Advanced IC Packaging Solutions and Reliability Challenges

Speaker: Dr. Richard Rao, Technical Fellow, Microsemi Corp.

July 24, 2018 at 6:30 PM

Location: Skyworks Solutions, Newbury Park, CA

This talk provides an introduction of most advanced IC packaging solutions and related reliability challenges. It covers 3D/2.5D/2.1D and FanOut WLP packaging integration, advanced interconnects such as TSV (Through Si Via) /uBumps, Si Interposer, Cu Pillar and Cu/Cu direct bonding related failure modes, and finally the Chip to Package Interaction (CPI) issues on 16 nm and beyond FinFET nodes.



Dr. Richard Rao is currently a Technical Fellow of Microsemi, a Microchip Company, a leading supplier of high reliability integrated circuits, located in Southern California and a Senior Member of IEEE. He is the present Chair of IEEE EPS (Electronics Packaging Society) Reliability Technical Committee. Dr. Rao is responsible for the corporate reliability and advanced packaging solutions. His focus is to find advanced packages to meet the high performance, high reliability and high-power semiconductor ICs; to study the new failure modes and mechanisms of cutting edge silicon and packaging technologies as well as to develop design for reliability solutions for advanced circuits, packaging and chip to package interaction. He has a Ph.D. degree in solid mechanics of materials from the University of Science and Technology of China. Prior to joining Vitesse Semiconductor Corp (now Microsemi) in 2004, Dr. Rao held various academic and technical positions in reliability physics and engineering. He was an associate professor at University of Science and Technology of China, a research fellow at Northwestern University, a National Science and Technology Board Research Fellow in Singapore; and a principal engineer at Ericsson Inc. He has published over 30 papers on reliability physics and applications and he is a main contributor of several JEDEC standards. He is a technical committee member of IRPS (International Reliability and Physics Symposium) and ECTC (Electronics Component and Technology Conference). He is a frequent speaker to IRPS, ECTC, ISQED (International Symposium on Quality Electronics Design), ASME Symposiums and a keynote speaker to ICEPT and International Conf on System on Chip, etc. Dr. Rao has over 20 years hands on experience and knowledge in silicon to package to system integration such as HKMG and FinFET, high performance FCBGA/CSP, WLP, 2.5D/3D, chip to package to board interaction, board and system level reliability physics and applications. He was invited to give keynote speech and tutorials on several international conferences.

Location

Skyworks Solutions

649 Lawrence Drive, Newbury Park, CA 91320

Intersection of West Hillcrest Drive and Lawrence Drive

(**NOT** the main building, please use link below to arrow that pinpoints building)

http://maps.google.com/maps?q=34.187542,-118.930994&num=1&t=h&vpsrc=0&ie=UTF8&z=18&iwloc=A

Directions

From Los Angeles

Highway 101 North
Take exit 47A for Rancho Conejo Blvd
Use the left lane to turn right onto Rancho Conejo Blvd
Turn left onto W Hillcrest Dr.
Destination will be on the right

From Ventura

Highway 101 South
Take exit 47B for Wendy Dr. toward Newbury Park
Turn right onto N Wendy Drive
Continue onto Camino Dos Rios
Turn right onto W Hillcrest Drive
Destination will be on the left.